

The listing of claims will replace all prior versions, and listings, of claims in the application:

**LISTING OF CLAIMS:**

Claims 1 - 46 (Previously Cancelled).

47. (Currently Amended) A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a second memory cell section including a second memory cell;

a first signal line connected to said first memory cell section;

a second signal line connected to said second memory cell section; and

a data circuit connected to one ends of said first and second signal lines, and including a capacitor and a latch circuit;

wherein first program /read data of said first memory cell is temporarily stored in said data circuit, and latched in said latch second program /read data of said second memory cell is held by said second signal line.

48. (Currently Amended) A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a second memory cell section including a second memory cell;

a first signal line connected to said first memory cell section;

a second signal line connected to said second memory cell section; and

a data circuit connected to one ends of said first and second signal lines, and including a capacitor and a latch circuit;

wherein

said first and second memory cells are programmed substantially simultaneously; and

~~while a program voltage is supplied to said second memory cell, program data of said second memory cell is held by said second signal line, and while said program voltage is supplied to said second memory cell, a verify read operation to verify whether said first memory cell has been programmed sufficiently, is carried out by said data circuit~~latch circuit, and while said program voltage is supplied to said first memory cell, a verify read operation to verify whether said second memory cell has been programmed sufficiently, is carried out by said latch circuit.

49. (Currently Amended) A nonvolatile semiconductor memory ~~comprising:~~according to claim 48,

~~a first memory cell section including a first memory cell;  
a second memory cell section including a second memory cell;  
a first signal line connected to said first memory cell section;  
a second signal line connected to said second memory cell section; and  
a data circuit connected to one ends of said first and second signal lines, and including a capacitor and a latch circuit;~~

wherein

~~said first and second memory cells are programmed substantially simultaneously;~~

~~while a program voltage is supplied to said second memory cell, program data of said second memory cell is held by said second signal line, and while said program voltage is supplied to said second memory cell, a verify read operation to verify whether said first memory cell has been programmed sufficiently, is carried out by said data circuit; and~~

~~while said program voltage is supplied to said first memory cell, program data of said first memory cell is held by said first signal line, and while said program voltage is supplied to said first~~

~~memory cell, a verify read operation to verify whether said second memory cell has been programmed sufficiently, is carried out by said data circuit.~~

50. (Currently Amended) A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a second memory cell section including a second memory cell;

a first signal line connected to said first memory cell section;

a second signal line connected to said second memory cell section; and

a data circuit connected to one ends of said first and second signal lines, and including a ~~capacitor and~~ a latch circuit;

wherein

said first and second memory cells are programmed substantially simultaneously;

while a program voltage is supplied to said second memory cell, program data of said second memory cell is held by said second signal line, and while said program voltage is supplied to said second memory cell, the program data of said first memory cell held by said first signal line is ~~transferred to said data circuit~~ latched in said latch circuit and a verify read operation to verify whether said first memory cell has been programmed sufficiently, is carried out by said ~~data circuit~~ latch circuit;

while said program voltage is supplied to said first memory cell, program data of said first memory cell is held by said first signal line, and while said program voltage is supplied to said first memory cell, the program of data said second memory cell held by said second signal line is ~~transferred to said data circuit~~ latched in said latch circuit and a verify read operation to verify whether said second memory cell has been programmed sufficiently, is carried out by said ~~data~~

~~circuit~~ latch circuit.

51. (Original) The nonvolatile semiconductor memory according to claim 47,  
wherein

said first memory cell and said second memory cell are connected to different word lines.

52. (Original) The nonvolatile semiconductor memory according to claim 48,  
wherein

said first memory cell and said second memory cell are connected to different word lines.

53. (Original) The nonvolatile semiconductor memory according to claim 49,  
wherein

said first memory cell and said second memory cell are connected to different word lines.

54. (Original) The nonvolatile semiconductor memory according to claim 50,  
wherein

said first memory cell and said second memory cell are connected to different word lines.

55. (Currently Amended) A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a first signal line connected to said first memory cell section;

a second signal line; and

a data circuit connected to one ends of said first and second signal lines, and including a  
~~capacitor and a latch circuit, said data circuit temporarily storing~~ latching program / read data;

~~signal lines, said data circuit temporarily storing program / read data;~~

wherein

said program / read data of said first memory cell is held by said second signal line.

56. (Currently Amended) A nonvolatile semiconductor memory comprising:

- a first memory cell section including a first memory cell;
- a first signal line connected to said first memory cell section;
- a second signal line; and
- a data circuit connected to one ends of said first and second signal lines, and including a ~~capacitor and a latch circuit, said data circuit temporarily storing~~ latching program / read data;

wherein

while a program voltage is supplied to said first memory cell, program data of said first memory cell is held by at least one of said first and second signal lines;

after said program voltage is supplied to said first memory cell, said data circuit is electrically connected to said second signal line and the program data of said first memory cell held by said second signal line is ~~transferred to said data circuit~~ latched in said latch circuit; and

a verify read operation to verify whether said first memory cell has been sufficiently programmed, is carried out using said program data ~~stored~~ latched in said data-latch circuit.

57. (Currently Amended) A nonvolatile semiconductor memory comprising:

- a first memory cell section including a first memory cell;
- a first signal line connected to said first memory cell section;
- a second signal line;
- a third memory cell section including a third memory cell;
- a third signal line connected to said third memory cell section;
- a fourth signal line; and
- a data circuit connected to one ends of said first, second, third and fourth signal lines, and

including a ~~capacitor and a~~ latch circuit, said ~~data-latch~~ circuit ~~temporarily storing~~latching program/read data of at least one of said first and third memory cells;

wherein

said first and third memory cells are programmed substantially simultaneously, program data of said first memory cell is held by at least one of said first and second signal lines, and program data of said third memory cell is held by at least one of said third and fourth signal lines while a program voltage is supplied to said first and second memory cells;

a verify read operation to verify whether said first memory cell has been sufficiently programmed, is carried out by said ~~data-latch~~ circuit, and program data of said third memory cell is held by said fourth signal line while conducting the verify read operation of said first memory cell; and

said data circuit and said fourth signal line are electrically connected to each other, after the program data of said third memory cell held by said fourth signal line is ~~transferred to~~latched in said ~~data-latch~~ circuit, a verify read operation to verify whether said third memory cell has been sufficiently programmed, is carried out using the program data of said third memory cell held by said ~~data-latch~~ circuit, and while conducting a verify read operation of said third memory cell, the program data of said first memory cell is held by said second signal line.

58. (Original) The nonvolatile semiconductor memory according to claim 57, wherein

said first and third memory cells are connected to a same word line.

59. (Original) The nonvolatile semiconductor memory according to claim 55, wherein

while said program / read data is held by said first or second signal line, a potential of a signal line adjacent to said first or second signal line is set at a fixed potential.

60. (Original) The nonvolatile semiconductor memory according to claim 59, wherein

said fixed potential is a ground potential or a power supply potential.

61. (Original) The nonvolatile semiconductor memory according to claim 55, wherein

said first and second signal lines are bit lines.

62. (Original) The nonvolatile semiconductor memory according to claim 56, wherein

while said program / read data is held by said first or second signal line, a potential of a signal line adjacent to said first or second signal line is set at a fixed potential.

63. (Original) The nonvolatile semiconductor memory according to claim 62, wherein

said fixed potential is a ground potential or a power supply potential.

64. (Original) The nonvolatile semiconductor memory according to claim 56, wherein

said first and second signal lines are bit lines.

65. (Original) The nonvolatile semiconductor memory according to claim 57, wherein

while said program / read data is held by said first, second, third or fourth signal line, a potential of a signal line adjacent to said first, second, third or fourth signal line is set at a fixed

potential.

66. (Previously Presented) The nonvolatile semiconductor memory according to claim 65, wherein said fixed potential is a ground potential or a power supply potential.

67. (Previously Presented) The nonvolatile semiconductor memory according to claim 57, wherein said first, second, third and fourth signal lines are bit lines.

Claims 68 - 81 (Cancelled).



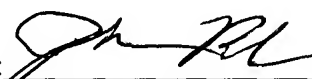
REMARKS

The present Amendment is provided as a submission in connection with a Request for Continued Examination filed herewith.

It is believed that no fee is required for this submission. If any fees are required or if an overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733 accordingly.

It is further believed that the publication fee listed in the Notice of Allowance paper is not required at this time. Nevertheless, should the publication fee be required to maintain pendency, then the Commissioner is authorized to debit our Deposit Account No. 19-0733 for the amount of the publication fee.

Respectfully Submitted,

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